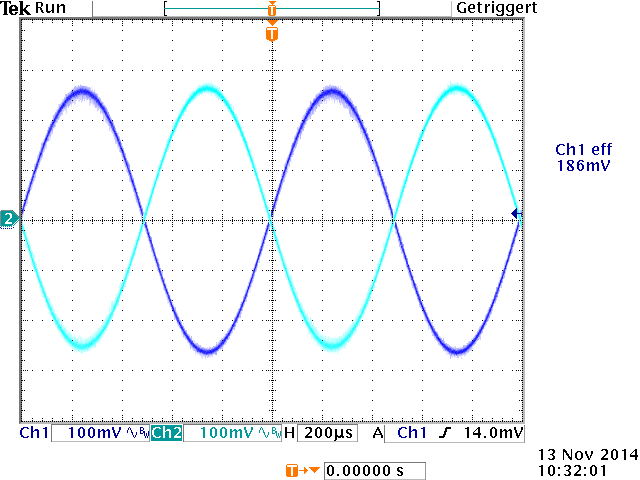
Offset voltage determined from the graph is **U0 = 5mV**

Slew rate (slope of the curve) S = ∆Ic/∆Ud

**S1 ≈ 0.02; S2 ≈ -0.02**

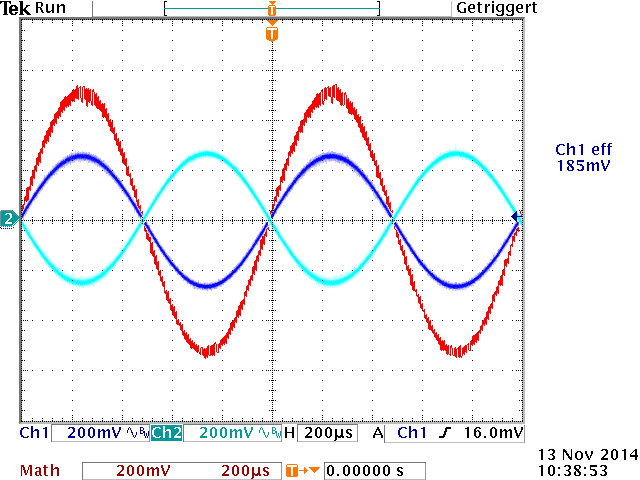
2 resistors Rc1 and Rc2, each 1 kΩ, are added in the Collector branches of the transistors. Alternating voltage UE eff = 10mV, f=1kHz is driven to the Base of T1. The voltages of both Collector terminals is given in the picture below.



Voltage values are the same **UR C1 = UR C2 ≈ 186 mV eff,** with 90° shift.

Single-ended voltage gain **Vu,se = UR/UE ≈ 186/10 ≈ 18.6**

The voltage between the 2 Collector Terminals is the difference between the voltages at each of them. Math function from the oscilloscope is used to calculate the difference.

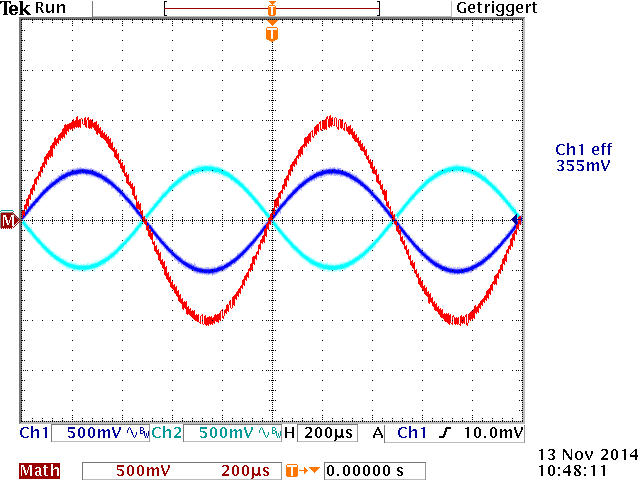


**Ua = UR C1 - UR C2 ≈ 185 – (-185) ≈ 370 mV eff** (the red curve from the graph)

**Differential voltage gain Vu,d = Ua/UE = 370/10 = 37**

Another resistor is connected in parallel with RE with the same value as RE (4.7 kΩ)

So the total resistance there is halved (0.5x4.7) hence the current I0 is doubled. The output voltage at Rc1 is measured and the voltage gain is evaluated.



**URc1 ≈ 355 mV eff**

**Vu,se = 355mV/10mV = 35.5**

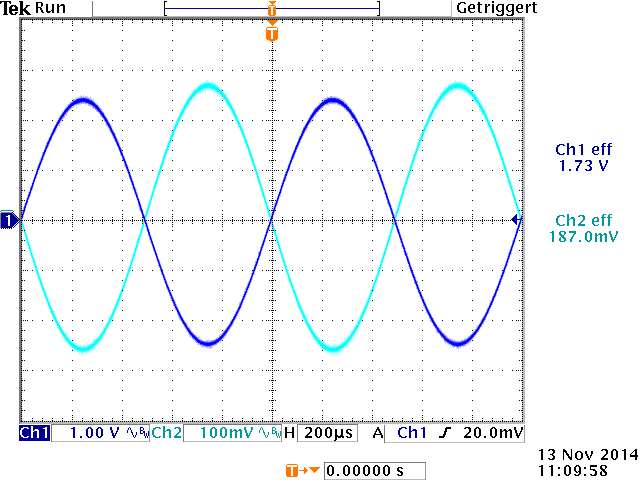
As we can see, doubling I0 leads to doubling the voltage gain:

At I0 => Vu,se ≈ 18

At 2\*I0 => Vu,se ≈ 36

Hence I0 is proportional to the voltage gain.

Both transistors’ bases are simultaniously supplied with input voltage UE and the output voltage at Rc2 is measured. The Common mode voltage gain is evaluated.



UE = 1.73 eff and the output voltage at Rc2 is 187 mV

**Vu,gl = URc2 / UE = 0.187 / 1.73 ≈ 0.11**

Common Mode Rejection Ratio (CMRR) is the ratio of the Differential voltage gain and the Common Mode voltage gain:

**CMRR = G = Vu,d / Vu,gl ≈ 37/0.11 ≈ 336**